REMARKS

Summary of Office Action

Claims 1-24 were pending in the above-identified patent application. Claims 11-24 have been withdrawn as being directed to an unelected invention.

Claims 1-10 were rejected under 35 U.S.C. § 102(b) as being anticipated by Owen et al. U.S. Patent No. 4,876,660 (hereinafter "Owen").

Summary of Applicants' Reply

Applicants have amended claims 1, 3, 7, 8, and 10 to more particularly define the claimed invention. Claims 11-24 have been cancelled without prejudice. The amendments are fully supported by the application as originally filed, and therefore no new matter has been added.

The rejections of applicants' claims are respectfully traversed.

Telephonic Interview Summary

On February 10, 2009, a telephonic interview took place between the Examiner and the undersigned. The undersigned wishes to thank the Examiner for the courtesies extended during the telephonic interview.

During the telephonic interview, the undersigned and the Examiner discussed the rejection of independent claims 1 and 8 under 35 U.S.C. § 102(b) as being anticipated by Owen. The Examiner agreed to further

consider the rejection upon receiving applicants' Reply to Office Action. Detailed arguments in support of applicants' position are presented below.

Applicants' Reply to the § 102 Rejection

The Office Action rejected claims 1-10 as being anticipated by Owen. Owen refers to a fixed-point multiplier-accumulator architecture. *See* Owen, Abstract. Owen's FIG. 6A shows a functional block diagram of an emmitter-coupled logic (ECL) multiplier-accumulator. *See* Owen col. 7, 47-61; col. 9, ll. 19-61; and FIG. 6A.

Applicants claimed invention is generally directed to methods for initializing or zeroing an accumulator value with minimal latency. As recited by applicants' amended independent claim 1, a first pair of input signals and a second pair of input signals are routed to circuitry that is concentrated in a particular area of a programmable logic resource. For example, the input signals may be routed to one or more multiplier-accumulator blocks. A multiply operation is applied to the second pair of input signals using the circuitry. A feedback output, which is initially set to zero, is applied to the circuitry. The first pair of input signals is concatenated. The feedback output is concatenated onto the end of the concatenated first pair of input signals. An accumulate operation is then applied to a result of the multiply operation and a result of the concatenating of the feedback output. A result of the accumulate operation is then stored for use as an initialized or zeroed accumulator value.

As recited by applicants' amended independent claim 8, a pair of input signals is routed to circuitry that is concentrated in a particular area of a programmable logic resource. A multiply operation is applied to the pair of input signals using the circuitry. A register is cleared in the circuitry based on at least one dedicated configuration bit that is set. A feedback output, which is initially set to zero, is applied to the circuitry. The feedback output is concatenated onto the end of the contents of the register. An accumulate operation is then applied to a result of the multiply operation and a result of the concatenating the feedback output. A result of the accumulate operation is then stored for use as an initialized or zeroed accumulator value.

Owen Does Not Concatenate Onto the End of
The Concatenated First Pair of Input Signals

Applicants have amended independent claim 1 to recite that the first pair of input signals is concatenated and then the feedback output is concatenated onto the end of the concatenated first pair of input signals. The Office Action contends that the feedback output is concatenated by adder 34 "with the result of the first sub-concatenating 32 bits and the initial 40 bit of zeros by MUX 56" of Owen's FIG. 6A (Office Action, page 5). A prior Office Action alleged that this claimed feature was shown by MUX 32 of Owen's FIG. 6A (July 3, 2008 Office Action, page 3). Applicants respectfully disagree and submit that neither MUX 32 nor adder 34 and MUX 56 of Owen's FIG. 6A shows applicants' claimed concatenating.

MUX 32 in Owen's FIG. 6A does not show concatenating any feedback output (which is initially set to zero) onto the end of the concatenated first pair of input signals, as recited by amended independent claim 1. The Office Action contends that the feedback output (i.e., a zero input to MUX 56) is fed into MUX 56, and the output of MUX 56 is connected to adder 34 (Office Action, pages 2-3). At no point, however, does FIG. 6A show concatenating the feedback output (which is initially set to zero) onto the end of the concatenated first pair of input signals.

Similarly, applicants' amended independent claim 8 also recites that the feedback output (which is initially set to zero) is concatenated onto the end of the contents of the register. As with independent claim 1, the Office Action contends that the feedback output is a zero input to MUX 56. This feedback output, however, is not concatenated with any register value. Rather, registers 14 and 16 are concatenated to form a 32-bit input to MUX 32. *See* Owen, FIG. 6A

Adder 34 also does not concatenate the feedback output onto the end of the concatenated first pair of input signals. Rather, adder 34 adds the output of MUX 32 and the output of MUX 56. As stated in Owen:

> In a 16 X 16 multiplier, this result includes 32 parallel bits consisting of sixteen least significant bits and sixteen most significant bits, each ordered from least to most significant bits. The result is input to a first or product input port 36 of an adder 34. A multiplexer function 32 selects, as the result to be input to the adder, either the product of multiplication, the result of concatenation, or zeroes. The adder has a second, accumulator contents input port 38. The result, and another binary number

> input via port 38 are added by adder 34 (Owen, col. 8, ll. 10-20).

As such, it is clear that although adder 34 may output 41 bits, adder 34 itself performs no concatenation. The only concatenation performed prior to adder 34 occurs just before MUX 32, where the 16-bit X operand may be concatenated with the 16-bit Y operand. MUX 32 may then output this concatenation, zeros, or the product of the multiplication from multiplier 30 (Owen, FIG. 6A). At no time does FIG. 6A show concatenating the feedback output (which is initially set to zero) onto the end of the concatenated first pair of input signals.

The Office Action further contends that the adder 34 shows concatenating of the "result of the first sub-concatenating 32 bits and the initial 40 bit of zeros by mux 56", since it is "adding 32 bit with 40 zero bits (e.g. equivalent to concatenating 32 bit with 8 zero bits)" (Office Action, pages 5-6). Applicants respectfully submit that this is different than the claimed feature of "concatenating the feedback output onto the end of the concatenated first pair of input signals" as recited by applicants' amended independent claim 1. Adding a 32 bit number with 40 zero bits would produce a result with 8 zero bits at the beginning of the 32 bit number. This is different than concatenating the feedback output (which is initially set to zero) onto the end of the concatenated first pair of input signals.

For at least the foregoing reasons, applicants submit that amended independent claims 1 and 8 are allowable over the prior art of record. Dependent claims

2-7, 9, and 10 are allowable for at least the same reasons. Applicants respectfully request, therefore, that the rejection of claims 1-10 under 35 U.S.C. § 102 be withdrawn.

Conclusion

Applicants respectfully submit that this application, including claims 1-10, is now in condition for allowance. Accordingly, prompt consideration and allowance of this application are respectfully requested.

Respectfully submitted,

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